

edaTrend DAC08

Collected EDA essentials in industry and business

Table of Contents and Example

DAC08
June 8-13, 2008
Anaheim, CA, USA



Imprint

„edaTrend DAC08“ was published in July 2008
by edacentrum GmbH.

edacentrum GmbH
Schneiderberg 32
30167 Hannover, Germany

Editors:
Dieter Treytnar, Peter Neumann, Ralf Popp

Authors: See page 66
Lecturer: Bill Murray, Daniel Payne
Design & Layout: Niklas Möller
Printed by Druckerei Hartmann GmbH, Germany

Thanks to all contributors to this report.

Copyright 2008 by edacentrum GmbH

All contributions to this „edaTrend DAC08“ report are subject to copyright. All rights reserved. No part of this book may be reproduced or transmitted in any form by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of the publisher. For information on getting such permissions, contact info@edacentrum.de.

Whilst every effort and care has been made to ensure the accuracy of the information in this publication, the publisher cannot accept responsibility for any errors it may contain. However, if this report contains any inapplicable information, a liability applies only for gross negligence.

The use of general descriptive names, registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

About edaTrend DAC08

The “edatrend DAC08” report summarizes the significant topics and trends at the 45th Design Automation Conference (DAC) in Anaheim, California. Because the DAC generates a huge amount of information, the “edatrend DAC08” report focuses on the essentials – the top events, such as keynotes and panel discussions. The report was compiled by edacentrum representatives, who personally attended these sessions.

The “edaTrend DAC08” report is divided into several sections: the first section contains general information about DAC 2008; the second section discusses the technical program (and the panel sessions in particular), and the third covers some DAC Pavilion panel sessions and other interesting meetings/events surrounding DAC. Section four consists of “wrap-ups” on verification and multi core design. “edaTrend DAC08” concludes with two short commentaries and the list of contributors.



Fig. 1: The Convention Center in Anaheim, CA, USA, place of the Design Automation Conference (DAC)

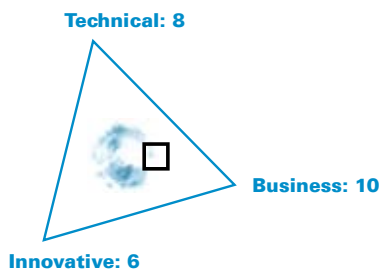


Fig. 2: No long distance to go in Anaheim, CA, USA – venue of DAC08

Content

Cold Rooms – Hot Topics at Anaheim	6
The Main Topic of DAC08 was Wireless	
Trend Report on the 45 th DAC – Design Automation Conference in Anaheim, California, June 8 – 13, 2008	
Step Back and Re-Think.....	9
Re-Thinking Analog Processes	
Plenary Keynote Justin R. Rattner – “EDA for Digital, Programmable, Multi-radios” June 10 th 2008	
The Future Will Be Wireless and EDA Is Needed as a Key Enabler.....	12
Lots of Technical Challenges Have to Be Solved under Difficult Market Conditions	
Plenary Keynote Sanjay K. Jha – “Challenges on Design Complexities for Advanced Wireless Silicon Systems” June 11 th 2008	
In the End it’s Math.....	15
How Model-based Design integrate Different Domains and Different Professions	
Plenary Keynote Jack Little – “Idea to Implementation: A Different Perspective on System Design” June 12 th 2008	
Parallel Computing is not the Holy Grail for EDA	18
Pros and Cons for EDA Going Parallel	
Session 8A – Panel: “Reinventing EDA with Many-Core Processors” June 10 th 2008	
What is the Next Multi-Core Silver Bullet?	22
The First Question of the Panel Remains Open	
Session 8B – Panel: “Multi-Core SoC Design is the Challenge! What is the Solution?” June 10 th 2008	
Electronic System Level: More Questions than Answers.....	24
Unsolved Issues Include Model Diversity, Verification, Legacy	
Session 18 – Panel: “ESL Hand-off: Fact or EDA Fiction?” June 10 th 2008	
Success is No Accident	27
How to Overcome the Wireless Integration Rally	
Session 21 – Panel: “Next Generation Wireless-multimedia Devices - Who is up for the Challenge?” June 11 th 2008	
Modeling the Unknown.....	30
Verification Using Mathematical Models vs. Physical Prototypes	
Session 30 – Panel: “Verifying Really Complex Systems: On Earth and Beyond” June 11 th 2008	
Thermal EDA Solutions are Used by Early Adopters	34
What will be Mainstream in Three Years?	
Session 36 – Panel: “Keeping Hot Chips Cool: Are ICThermal Problems Hot Air?” June 11 th 2008	
DFM Value Depends on Where You Need to Add Value	37
Hit or Hype? What Adds Value? What Doesn’t?	
Session 48 – Panel: “DFM in Practice: Hit or Hype?” June 12 th 2008	
How to Make Custom Fall in Love with Synthesis.....	42
A Lively Debate About Synthesis vs Custom	
Session 54 – Panel: “Custom is from Mars and Synthesis from Venus” June 12 th 2008	
No Bragging, Just Facts	44
Challenges for 2011	
Pavilion Panel 6: “Will 22 nm Be Our Catch-22?” June 9 th 2008	
Problems Faced - Solved by Collaboration	46
45 nm: Altogether Now	
Pavilion Panel 7: “45nm: Collaborate, Aggregate, Differentiate” June 10 th 2008	
For a Few Dollars More	48
Profitability and Future Business of IP	
Pavilion Panel 10: “IP Selection: The Good, The Bad, and The Ugly” June 10 th 2008	
The Good, the Bad and the Ugly Experiences with Low Power	50
About the Dream of a Holistic, Consistent and Automated Design Flow	
Pavilion Panel 15: “Advanced Low Power Techniques: Is Your Design Method Too Powerful?” June 11 th 2008	
Gary Smith Reads the Tea Leaves.....	52
Significant Trends Plus What’s Hot@DAC	
Sunday Pre DAC Gary Smith on EDA June 8 th 2008	
No Real Common Ground, But ESL Is Here!	54
Users Categorize ESL Into Verification, Analysis And Design, Resulting In A \$200M Market	
Workshop: ESL Symposium June 11 th 2008	
DAC and Verification - an Oxymoron?.....	56
Brian Bailey on Verification at DAC 2008	
Time to start counting! Cores, that is!	59
Grant Martin on Multi-Core and Many-Core at DAC 2008	
Looking Back at DAC.....	62
Some constrained-random observations	
A guest commentary by Bill Murray	
Alive and Kickin’.....	64
Living in Interesting Times	
edacentrum Commentary	
About us	66
edaTrend authors and edacentrum	

The Future Will Be Wireless and EDA Is Needed as a Key Enabler



Lots of Technical Challenges Have to Be Solved under Difficult Market Conditions

Plenary Keynote

Sanjay K. Jha – “Challenges on Design Complexities for Advanced Wireless Silicon Systems”

June 11th 2008

Keywords: Fabless, Wireless, Co-Development, Business Models

Abstract

The global wireless landscape continues to change as demand for 3G technology accelerates. Huge markets offer huge opportunities for semiconductor companies, but the characteristics of these markets and the technical issues to be solved lead to a lot of serious challenges.

Dr. Sanjay Jha, from Qualcomm addressed all of these future trends in his keynote, including the role of collaboration in product development, plus the kind of support and products required from the EDA industry and how business models might look.

Keynote Content

Keynoter Sanjay Jha explained what a fabless semiconductor provider has to deliver in order to satisfy his customers. As Qualcomm is the No. 1 wireless chipset provider, everybody listened carefully to his advice. He pointed out that technical features are of fundamental importance, but increasingly crucial is the value the product offers to the user. This value is not only a question of features, it is strongly connected to personal feelings the user associates with this product.

While each delivery has to include all the tools and all IP, it is important to make technology hidden but accessible, Jha pointed out.

“What matters is what we deliver”

Sanjay Jha, Qualcomm

Talking about the future of electronics and of wireless in particular, Jha focused on his three major growth-drivers: emerging markets, broadband and converging applications.

Growth-driver No. 1 is to serve emerging markets like India, China, Africa etc. For these huge markets, projected at more than 9 billion users, nobody is going to consider solutions based on copper wires, the choice will be wireless. Cur-



Fig. 1: Dr. Sanjay Jha, Qualcomm

rently there are 5-7 million new subscribers to wireless services per month in China - that means that the number of new subscribers annually in China exceeds the total number of subscribers in the USA. In India wireless applications have already outpaced wired applications.

However, the price at which new customers can afford to buy is getting lower and lower (despite an increased list of features, which cannot be reduced for these markets). The number of potential customers in China and India is huge, but the majority of them cannot afford to spend more than 15-20 \$ for such a product. In Europe the average selling price (ASP) is around 140 \$ today.

Growth-driver No. 2 will be that wireless is becoming broadband. Wireless applications migrate from pure voice to all kinds of data trans-

Overall impression



Good and insightful keynote

Dr. Sanjay Jha, Qualcomm CDMA Technologies

Dr. Sanjay Jha is chief operating officer of Qualcomm and president of Qualcomm CDMA Technologies (QCT), the world's top wireless chipset provider and largest fabless semiconductor producer. He is also a member of the Qualcomm Ventures advisory committee. Dr. Jha has also served as chairman of the Fabless Semiconductor Association. This is the voice of the fabless business model and a group with more than 450 corporate members, now known as the Global Semiconductor Alliance (GSA).

mission. Providing the necessary bandwidth for the data services will be key.

Growth-driver No. 3 will be the convergence of consumer electronics and mobility. According to Jha the future of mobile devices will be a PCD (Pocketable Computing Device) in every pocket, with features including gigahertz processors, video capabilities and high resolution touch screens. When you come home you dock the PCD, mostly by connecting it by wireless to your home-devices.

The overall global demand for handsets will remain strong across multiple segments despite economic slowdown, Jha summarized. The average selling price is falling fast, especially for the high-priced items.

Then Jha moved to more technical issues. The technical challenges are numerous with power consumption as one of the most burning ones. Required are 6-8 hours of usage and several weeks of stand-by. This is getting harder and harder to reach, as the capacity of batteries increases only within 5-7% per year, which is far



Fig. 3: Dr. Sanjay Jha, Qualcomm together with the 'magic 45' of DAC



Fig. 2: The audience listened to the keynote

from being enough. As people prefer nice graphics and pictures on high-resolution displays over simple text messages, the display has become the dominating power consumer.

Wireless devices will not only include a digital camera and digital video in high quality, they will also serve as displays for external functionality. But, as Jha pointed out: A device which doesn't fit in your pocket will not make it.

Finally, Jha highlighted two major points where help is required from the EDA industry: co-development of Hardware/Software and co-design of dies, packaging and systems.

According to Jha, co-development of hardware and software still is a challenge, thus he called for Hardware/Software concurrent design tools. Time and cost for the development of the software parts of a SoC for mobile devices is an issue, but also the insufficient co-operation between hardware and software design when working on energy management techniques.

As everything Qualcomm ships today is either an RF/mixed-signal SoC or a multi-die package as Jha explained, he requests tools that enable co-design of dies, packaging and systems. Designers should be able to model the package and the placement of key components like displays and antennas in an early stage of the design flow. More automation and better package parasitic extraction are needed. Today the integration of the design is still troublesome.

The audience clearly understood Jha's concerns, but was also aware of the high cost involved in the development of such tools, which only a few customers can afford. So he was asked if he could imagine collaborating with EDA vendors on a royalty base. Jha was a bit reluctant, but said that he would be willing to discuss royalties, if

the value offered by the tool is substantially high. However, the threshold to be passed is very high; for example a piece of IP which might be developed by themselves in a couple of months would be far away from that.

Finally, the discussion touched the question of fair allocation of profits in the electronics industry. Jha sees over-competition and a need for consolidation in the semiconductor industry. He pointed out that even though the concepts for great products are developed by the semiconductor industry, they only get a share of 5-7% of the average selling price (ASP) of the final product. According to Jha they would deserve much more, but they don't control things like branding and distribution which influence the ASP directly. In the end, Jha and his suppliers from the EDA industry are at different stages in the food chain but face similar problems.

Summary

Due to emerging markets Jha predicts that broadband and converging applications will create huge growth rates for the wireless market. Lots of technical challenges have to be solved in order to satisfy the requirements of this market, including EDA tools for co-design of hardware and software, but also of dies, packaging and system. Both industries, semiconductor as well

as EDA, have problems in getting a reasonable share of the ASP of the final product.

Commentary

Jha provided lots of interesting insights into Qualcomm's business, the upcoming opportunities in the wireless market and the technical challenges associated with them. He also translated these challenges into business opportunities for the EDA industry. However, he did not present new concepts for financing new EDA solutions.

Links

- Qualcomm: www.qualcomm.com
- "Qualcomm COO outlines 'smart phone' challenges" SCDSources: www.scdsource.com
- "Latest from DAC: Qualcomm COO Jha offers advice -and a deal -to the EDA industry" EDN Blog: www.edn.com/blog/1690000169/post/850028085.html

Author

[Jürgen Haase](#), [edacentrum](#)

About us



Dr. Jürgen Haase is Office Director of edacentrum e. V. since 2001, and manages the office of edacentrum in Hannover. Prior to this, he worked for the Institute for Network- and SystemTheory at the University of Stuttgart; Philips Communications Industry AG in Nürnberg; and Sican GmbH/sci-worx GmbH in Hannover, on digital video communications, optical telecommunication systems, and ASIC/SoC design. He has been active in a significant number of international R&D projects, and has managed the design of numerous ASICs for customers based in Europe, the U.S. and Asia. (haase@edacentrum.de)



Dr. Cordula Hansen received her Dipl.-Inf. degree in Computer Science in 1993 from the University of Karlsruhe (TH), Germany. From 1993 to 1995, she worked for the German EDA company ISDATA, where she was responsible for the development of VHDL synthesis tools. From 1996 to 2001, she worked for the Research Center for Information Technologies (FZI) in Karlsruhe and in the Department of Computer Engineering at the University of Tübingen, where she received her Ph.D. in 1999. Her research specialties included high level synthesis and test bench generation. In 2001, Cordula joined edacentrum, where she is responsible for R&D project consulting, product development and process management. (hansen@edacentrum.de)



Peter Neumann holds a B. Eng. (Hons.) degree in Computer and Information Engineering from London South Bank University, and a Dipl. Ing. (FH) in Electronic Engineering from Fachhochschule Bremen. He has worked for more than a decade in industry in various digital design areas, including design flow, IP qualification, chip design and verification, and top-level SoC integration. He has spent the last two years in the field of configurable processors. In 2007, Peter joined edacentrum, where he is responsible for business development. (neumann@edacentrum.de)

edaTrend authors and edacentrum



Ralf Popp received his Dipl.-Ing. degree in Electrical Engineering in 1996 from the University of Hannover, Germany. From 1997 to 2002, he worked at the Institute of Microelectronic Systems, University of Hannover, in the computer-aided design of analog circuits. His primary specializations were the symbolic analysis, behavioral modeling and simulation of analog and mixed-signal circuits, a field in which he is currently writing his Ph.D. thesis. In 2002, Ralf joined edacentrum, where he is responsible for technical analyses, public relations and marketing. (popp@edacentrum.de)



Susanne Sass received her Dipl.-Ing. in Electrical Engineering in 2006 from the University of Hannover, Germany. Her primary specialization was technical computer science/computer engineering. Her diploma thesis focussed on developing a hardware/software environment to analyze the status of a real-time operating system. In 2007, Susanne joined edacentrum, where she is responsible for the management and coordination of research projects. (sass@edacentrum.de)



Dr. Volker Schöber received his Dipl.-Ing. in electrical engineering in 1991, from the University of Hannover, Germany. From 1991 to 1996 he was a research assistant at the University of Hannover in the field of design for testability (DFT) of ICs. He received his Ph.D. in computer science in 2000 from the University of Hannover. He also worked for Siemens Semiconductor and Infineon Technologies from 1997 until 2002. Since 2002, he has worked for the edacentrum, where he is responsible for cluster research projects. Since 2005 he has been a lecturer in the test of integrated circuits and systems at the University of Hannover. (schoeber@edacentrum.de)



Dr. Dieter Treytnar received his Ph.D. in Electrical Engineering in 2005 from the University of Hannover, Germany. His thesis was entitled „The influence of parasitic effects in nanometer interconnect systems on the digital test pattern quality“. From 1997 to 2002, he worked at the Institute of Electromagnetic Theory and Microwave Technique, University of Hannover, on the problems of signal integrity and test of deep submicron design arising from the interconnect between cores. In 2002, Dieter joined edacentrum, where he is working in public relations and marketing and is responsible for the management of EDA research projects. (treytnar@edacentrum.de)



Dr. Andreas Vörg received his Dipl.-Ing. in Electrical Engineering with a specialization in technical information processing in 2000, from the University of Karlsruhe, Germany. He received his Ph.D. in Computer Science in 2005 from the University of Tübingen, Germany. Since 2000, his primary field of interest has been the automated qualification and delivery of reusable intellectual property (IP) components. In 2005, Andreas joined edacentrum, where he is responsible for EDA consulting services and the management of EDA research projects. (voerg@edacentrum.de)



The edacentrum is an independent organization dedicated to the promotion of research and development in the area of electronic design automation (EDA). Its main role is to initiate, evaluate and supervise industry driven EDA R&D projects and to provide individual services in the EDA sector. Further by encouraging cluster research projects and EDA networks, it bundles and reinforces the EDA expertise of universities and research institutes.

The edacentrum provides individual services in the EDA sector, including consulting, project management, the organization of trainings, workshops and networking events and provides a communication platform to the EDA community.

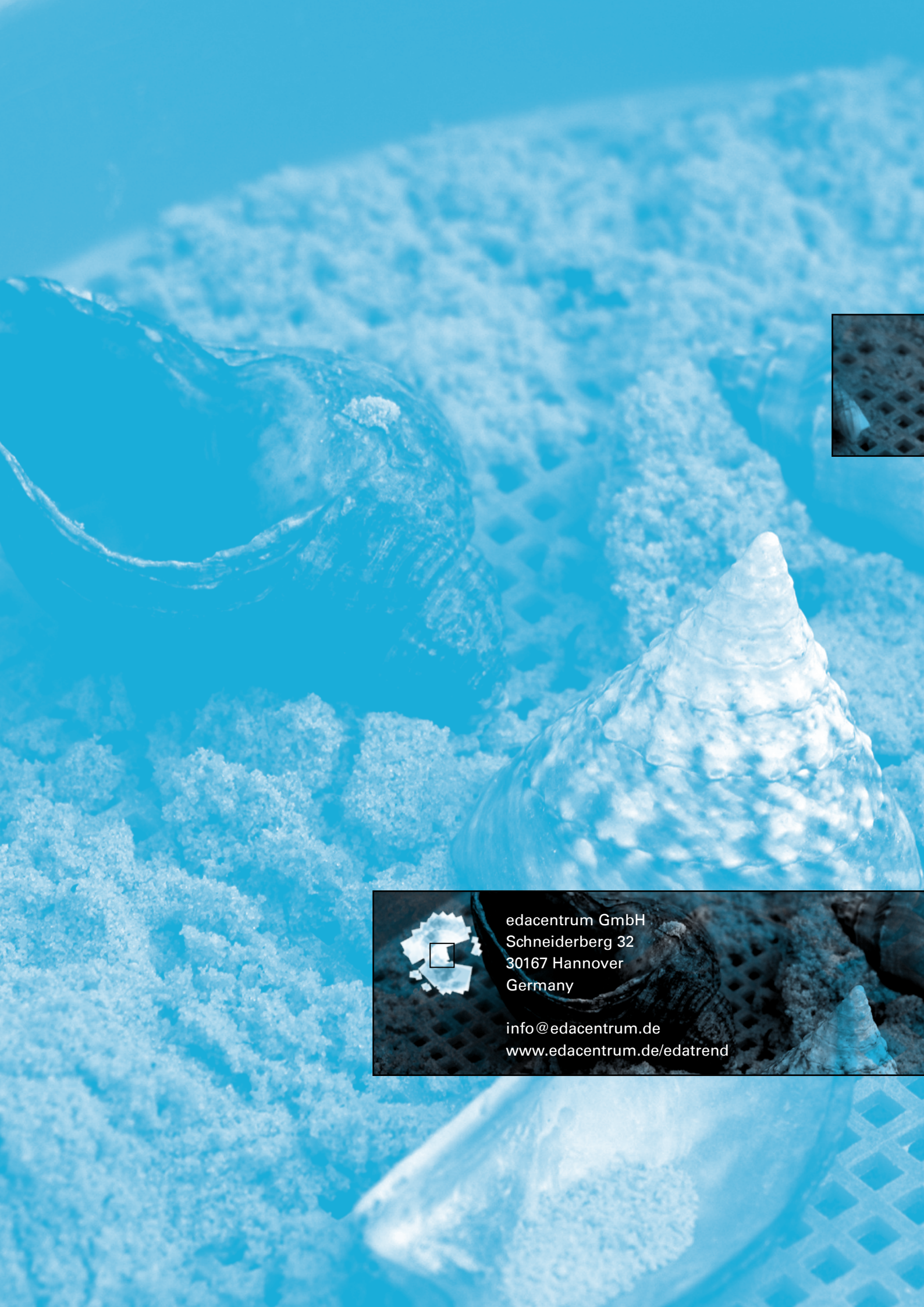
Dr. Klaus Winkelmann has more than 20 years of industry experience in applied computer science. His main area of interest is formal verification. After managing R&D projects at Siemens Corporate Technology and Infineon Technologies, he joined OneSpin Solutions in 2005. His current responsibility is Technical Marketing for OneSpin's functional verification technology.

Frank Schirrmeister is director, product management at Synopsys, responsible for the system-level products Innovator, DesignWare® System-Level Library and System Studio, with a focus on virtual platforms for early software development. Prior to joining Synopsys, Frank held senior management positions at Imperas, ChipVision, Cadence, AXYS Design Automation and SICAN Microelectronics. Most recently, he served as VP of marketing at Imperas, a provider of solutions for multicore software development. At Cadence he served as group director of verification marketing in the Design and Verification Business Unit and was instrumental in market introduction and proliferation of innovative products such as Virtual Component Co-Design, Verification Cockpit and Incisive. Frank has authored 60+ publications and now also runs the system-level blog "A View from the Top" at <http://www.synopsysoc.org/viewfromtop/>

Paul Cohen has over 30 years of experience in the IC and EDA industries. After spending many years as an IC designer using various EDA tools, he moved to the EDA world as an applications and technical marketing engineer. Prior to joining the EDA Consortium, Paul was a Corporate Applications Engineer at Virage Logic. In his current role as a Member of the Technical Staff at the EDA Consortium, he is involved in many of the Consortium's operations.

The edacentrum actively engages in public relations in order to sensitize higher management levels, the public and the political arena about the central importance of design automation in solving the system and silicon complexity problems in microelectronics.

The edacentrum consists of an association (edacentrum e.V.) and a company (edacentrum GmbH). The association operates on behalf of its members and the projects supported by it and actively engages in public relations for EDA. The company provides individual services in the EDA sector. At present more than 50 companies are member of the edacentrum e.V. The association is open to all persons and legal entities.



edacentrum GmbH
Schneiderberg 32
30167 Hannover
Germany

info@edacentrum.de
www.edacentrum.de/edatrend